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Welcome to the 2014 Engineers’ Guide to PCI Express Solutions

As Extension Media’s Chris Ciufo says, the PCI-SIG is one industry consortium that doesn’t let the grass grow under its feet. Chris took a deep dive into the PCI-SIG’s most recent PCI Express announcements (made earlier this year), and looks ahead as well. You won’t want to miss his insight in “PCI-SIG ‘nificant’ Changes Brewing in Mobile” where he covers everything from the PCIe 3.1 spec through expectations for 4.0, as well as the M.2 and M-PCIe specifications that are aimed squarely at the exploding mobile markets. We also looked to our industry experts to get their take on these changes and more, in our roundtable discussion, “PCI Express Moves Outside the Box.”

In other articles, Pericom’s Rakesh Bhatia explains how PCIe supports connectivity with legacy equipment built on interfaces that are all but obsolete in “Bridging Legacy Equipment with PCIe.” Agilent’s Rick Eads addresses the complex task of testing PCI Express transmissions—and how that will only get tougher with the upcoming Gen 4 release. In his article, “Switching Simplifies PCI Express Testing,” he explains how switches can not only speed up measurements, but can also provide results that compare favorably or even exceed current test practices. And because USB 3.0 and PCIe share some common specifications, we’ve included Eric Huang’s (Synopsys) article, “The Accelerating Demand for 10 Gbps SuperSpeed USB 3.0.”

Elsewhere in this issue, you’ll find more information on how this popular standard takes high-performance into a range of embedded applications. CES’s Akos Csilling looks at the advantages of PCI Express for traditional VME-based applications in “Modern Technology in a Traditional Form Factor,” while Emerson’s Brian Carr explains how a PCI Express media processing accelerator card offers benefits for high-density voice and video processing in “Accelerate Server-based Media Processing.” Finally, GE’s Peter Thompson explains how multiprocessing—and PCI Express—are at the heart of high-performance embedded computing in mil/aero systems with significantly improved performance in “Multiple Processors in High-Performance Embedded Computing: “Only Connect”. “

There’s all this, plus product information, news, white papers and more, so dig in and enjoy!

Cheryl Berglund Coupé
Editor

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PCI Express Moves Outside the Box

Our roundtable discussion hits PCIe’s generational shifts to address demanding requirements, the outlook for the new PCIe OCu-Link cable, and the move to mobile and low-power applications.

By Cheryl Coupé, Managing Editor

It’s tough to limit a discussion on PCI Express, as the standard continues to evolve into nearly every aspect of computing. New generations will support highly demanding applications in the data center as well as remote exploration, surveillance and research equipment that collect and process large amounts of data before they can be transported for the next level of processing. And new efforts are taking the standard out of the box to cable, mobile and small form factors. John Wiedemeier, senior product marketing manager for Teledyne LeCroy and Larry Chisvin, vice president of strategic initiatives for PLX Technology were kind enough to offer their views on these topics and more.

EECatalog: How are the different PCI Express (PCIe) versions being implemented in embedded systems today? Do you expect that to change?

John Wiedemeier, Teledyne LeCroy: Historically, the embedded market has been more conservative to adopt higher speeds into their systems. Many of the embedded products are satisfied with their performance but looking for competitive differentiators that can add more product value. Improving I/O performance is a sure way to do that. Definitely, we are seeing companies transition from PCIe Gen1 (2.5GT/s) to Gen2 (5GT/s). Most embedded companies seem content for now at PCIe 2.0 and have not moved to the higher-speed PCIe 3.0 standard. New opportunities with PCIe-based storage and lower pricing on fast PCIe-based CPUs will certainly be game changers in the near future.

Larry Chisvin, PLX Technology: PCI Express has been a part of embedded design since the specification was first released, largely due to its software compatibility with PCI, which had already permeated the embedded world. PCIe offers low cost, high performance and flexibility, and since embedded systems are largely built with the same components used in other, higher-volume markets, PCIe is an ideal way to connect together the components inside embedded systems. As with most of the industry, PCIe Gen 2 has been broadly adopted, and Gen 3 is showing up in newer systems. Since embedded platforms have long lives, designers tend to use components that will not soon be obsolete, but at the same time the components must have an established track record of quality; embedded systems almost never crash. So earlier generations of PCIe are used where the performance is adequate, and newer versions where the trade-off pushes the designers toward additional performance.

PCIe has been adopted in many standards developed for the embedded industry, such as PICMG 3.4 for the ATCA chassis and VITA 41 & 46 specifications for various connectivity and switch fabric applications. This is likely to continue, as each version of PCIe has full backward compatibility of software and firmware for a seamless and easy migration experience. PCIe Gen 3 allows for advanced applications, such as a PCIe switch-based fabric, such as PLX’s Express-Fabric, that allows for unprecedented consolidation, convergence and power-savings in data centers and cloud environments, thanks to the reduced need for components and board space.

Using PCIe instead of Ethernet for short-distance, rack-level communication can offer substantial cost and power advantages, and this will continue to be the case as PCIe moves to Gen 4.
Ethernet will have its place connecting networks and data centers to the cloud providing carrier Ethernet-based services. PCI Express 4.0 with its doubling of performance and low latency will build the next-generation infrastructure of networked servers and storage systems. Protocol analysis will become important as developers work to achieve quality products and overcome issues related to these big changes in this new specification.

Chisvin, PLX Technology: As with every version of PCIe, the first implementations will show up in the graphics and high-end server markets, where either the bandwidth is necessary or the application is able to command a substantial premium. This will be followed quickly by the storage market, where ultra-high-performance SSD-based systems will strain the capabilities of the fabric and backbone. Over time, Gen 4 will migrate to the general-purpose data center and cloud markets, as the components being connected together continue to push the need for greater interconnection speeds.

Overall, this will not impact Ethernet in a major way, since there is an infrastructural advantage that Ethernet has developed, and since the Ethernet suppliers are also pushing their performance higher for the same reasons. In fact, PCIe and Ethernet are highly complementary of one another; they already coexist in a wide range of systems across several market segments. The one area that Ethernet will be impacted is inside the rack of a data center or cloud provider, and this has already started. Using PCIe instead of Ethernet for short-distance, rack-level communication can offer substantial cost and power advantages, and this will continue to be the case as PCIe moves to Gen 4.

PCIe Gen 4 is not expected to be deployed in the applications above before the 2016-17 timeframe, but when it does appear it will be utilized in the same manner as current PCIe generations, but twice as fast. Applications that could benefit from Gen 4’s higher speed are future unmanned aerial vehicles, space/atmosphere research and undersea/underground-exploration equipment that need to collect and process large amounts of data before they can be transported for the next level of processing. Additionally, unmanned air (ground and underground) vehicles in commercial applications will be a prime target for PCIe, both Gen 3 and Gen 4.

**EECatalog:** Where do you anticipate seeing implementations of PCI Express 4.0, which will boast 16 GT/s (at 16 Gbps) or about 64GB/s (x16)? Will it give Ethernet any cause for concern?

**Wiedemeier, Teledyne LeCroy:** The demand for cloud computing with its infinite networked virtualized data storage is driving I/O performance. PCI Express 4.0 at 16GT/s will deliver the speed and performance required to meet these challenges. High-speed interconnects at these data rates will drive faster servers and high-capacity SSD-based storage systems.

**EECatalog:** PCI Express is planning for an expansion outside the box using a low-cost cable that the PCI-SIG says will rival Apple’s Thunderbolt for external devices, and can be used as a PCIe 32Gbps simplex (4-lane) bus extender. What are your predictions for the PCIe OCuLink cable?

**Wiedemeier, Teledyne LeCroy:** There are tremendous advantages to adopting the PCIe OCuLink cable besides speed. For one, a proprietary controller chip is not required to enable this to work with systems that use a PCI Express CPU-based system board.

This will allow system vendors to provide faster and more cost-effective products to market. However, with all of its merits, if the PCIe community does not rally around this new standard it will not gain the same visibility as Thunderbolt. I think this cable has a lot of potential with storage systems. It will provide the needed throughput to support the new high-capacity SSDs in storage and server systems.

**Chisvin, PLX Technology:** There are attractive reasons for taking PCIe out of the box, and key among the advantages is that the software model is vastly simplified when the system does not need to worry about where the devices reside physically. For example, performance suffers—and complexity increases—when data communicates on a motherboard using PCIe, then needs to be translated to Ethernet for transmission to another box, then translated back to connect up to all of the components. By keeping the data in its native PCIe form, the protocol translation overhead is reduced and meaningful performance improvement can be achieved. If the OcuLink cable can achieve its price targets, it should be very successful, since it will provide the ability to offer the advantages outlined. Of course, you can get most of those same benefits today by using existing PCIe, QSFP or miniSAS-HD cables, running the PCIe protocol across them, though at a higher cost.

**EECatalog:** As every version of PCIe, the first implementations will show up in the graphics and high-end server markets, where either the bandwidth is necessary or the application is able to command a substantial premium. This will be followed quickly by the storage market, where ultra-high-performance SSD-based systems will strain the capabilities of the fabric and backbone. Over time, Gen 4 will migrate to the general-purpose data center and cloud markets, as the components being connected together continue to push the need for greater interconnection speeds.
PCle OcuLink will offer active, passive and hybrid copper and optical cabling. The user will be able to select the cabling that suits the cost targets of the application they are serving. OcuLink, being an open standard, will allow volume manufacturers to build cables that are competitive in cost.

**EECatalog:** The forecasts show the PC market is shrinking—whether in units delivered, processor forecasts or most recently, the number of GPUs forecast. With the PC goes PCI Express, so the PCI-SIG’s M-PCle technology is focusing on mobile markets, including smartphones, tablets and portable embedded. What are the technical challenges (and upsides) to extending PCI Express into mobile?

**Wiedemeier, Teledyne LeCroy:** There are two challenges that had to be addressed for PCI Express to move successfully into the mobile market. The first challenge was to conquer PCI Express’s ability to operate in low-power designs where long battery life is essential. M-PCle is able to solve this by replacing the PCIe PHY with the new MIPI Alliance’s M-PHY. The low-power M-PHY provides proven power efficiency to enable low-power designs for mobile.

The second challenge was how to migrate the existing PCI Express software infrastructure in current PCI Express designs to the newer power-efficient architecture of M-PCle. M-PCle preserves the same upper protocol layers of PCIe, making it possible to do this. Maintaining the link and transaction layers as in the old PCIe programming model allows legacy software structure to easily port to the new M-PCle programming model. Teledyne LeCroy has recently provided for free a new software utility for M-PCle applications that will help developers view and edit their M-PCle devices configuration space registers. Providing tools to this new industry will help insure a successful transition for developers to this low-power architecture.

**Chisvin, PLX Technology:** I would challenge the belief that the success of PCIe is dependent on the PC market. That being said, expanding the total available market is always a good thing. The main challenge to using PCIe in the mobile market has been power, and that is what is being addressed by the PCI-SIG with the introduction of numerous enhancements to the protocol. By offering a power-efficient way to use PCIe in mobile devices, a new and large market opportunity has been created.

**EECatalog:** Small form factors are all the rage, in flavors ranging from PCIe/104 and AdvancedMC, to Gumstix and COM Express. The PCI-SIG’s M.2 spec is targeting ultra-light (think Ultrabooks) and ultra-thin (think tablets) devices. What are your thoughts on this new mobile-focused form factor?

**Wiedemeier, Teledyne LeCroy:** The new M.2 form factor is a great way to use SSD technology in thin-computing appliances where size and connectivity are restrained. M.2 devices will start out with Socket 2 (SATA Express x2) based devices and eventually move to Socket 3 higher performance M.2 devices later. From a test equipment perspective, Teledyne LeCroy is highly involved with providing ways to test new devices like this. Recently, we introduced an interposer for our PCIe protocol analyzer to support testing M.2 devices. Socket 2 and Socket 3 type M.2 devices which support SATA Express or NVMe can be connected to and analyzed for protocol correctness and performance.

**Chisvin, PLX Technology:** As is the case with the M-PCle protocol, extending PCIe’s ability to fit into highly dense applications in a standard way enables the technology to be used in places that had previously been excluded. Since almost every component already connects to its neighbors through PCIe, the new connector standard matches well with device packaging technology that has allowed highly compact consumer devices.

In the case of M.2, one of the most exciting usage models will be high-performance, low-power, flash memory-based storage that eliminates the need for the rotating media, thus dramatically reducing power needs and extending battery life.

Cheryl Berglund Coupé is editor of EECatalog.com. Her articles have appeared in EE Times, Electronic Business, Microsoft Embedded Review and Windows Developer’s Journal and she has developed presentations for the Embedded Systems Conference and ICSPAT. She has held a variety of production, technical marketing and writing positions within technology companies and agencies in the Northwest.
Bridging Legacy Equipment with PCIe

PCIe supports connectivity with legacy equipment built on interfaces such as RS-232 and PCI that are “obsolete” in the consumer electronics world.

By Rakesh Bhatia, Pericom

For many applications, product life is measured in years or decades. This trend is common among industrial and medical applications, as well as any industry where product longevity is expected. As a result, a technology disconnect can arise between long-life equipment and the tools used to interface to or control them.

For example, a machining center deployed in the ‘90s and still in operation today is most likely outfitted with a UART-based port such as RS-232 for data uploading and diagnostics. However, PCs and laptops no longer ship with an available RS-232 port. To continue to support legacy equipment with new software and diagnostic tools, OEMs need to be able connect equipment using current technology.

Note that this disconnect continues to be an issue even as equipment evolves. In many cases, the UART interface was replaced with a newer interface such as USB or PCI, commonly known as “conventional PCI” today. PCI in turn has been replaced by PCI Express (PCIe), so even PCI-based equipment can be difficult to connect to with current computing platforms. This article will address how OEMs across industries can use PCIe to support connectivity with legacy equipment built upon interfaces like RS-232 and PCI that are “obsolete” in the consumer electronics world.

Even with a PCIe plug-in card that does not require a cable, signal integrity can still be an issue.

Figure 1a and 1b show two basic architectures for a legacy bridge. The UART output from the system or piece of equipment is routed to a bridge, bridged to PCIe and then routed to the control point, typically a PC, laptop or diagnostic tool.

The bridge can either be a standalone box that connects to the control point via a cable or be integrated onto a PCIe card that plugs directly into the control point.

Today, bridging circuitry is available as an integrated component. A robust legacy bridge, however, requires more than simple conversion between interconnects. Through the use of switching technology, the flexibility and efficiency of a legacy bridge can be significantly improved, leading to overall lower operating costs and simplified system management. Signal conditioning can also be introduced to improve signal integrity and ensure system reliability under all operating conditions. Finally, a low-jitter timing source can ensure increased signal margin to ease design complexity.

Flexibility and Efficiency

Multiplexing enables two common ways to increase the flexibility and efficiency of an adapter bridge: through consolidating input ports and by supporting multiple output types. Consider applications such as in a hospital or on a factory floor, where several pieces of equipment are being monitored and/or controlled. Rather than have a separate converter for each piece, a single bridge can service multiple stations.

Given that PCIe offers substantially greater data rates than UART-based interconnects, one PCIe stream can...
easily accommodate several UART streams. Integration at the IC level enables a single multi-port bridge chip to perform the work of several individual bridges. For example, in Figure 2, a 4-port UART-to-PCIe bridge reduces the design footprint.

Consolidation offers many cost benefits. Rather than having to purchase multiple convertors, technicians only require a single convertor to support several end points. As a consequence, fewer control points are required as well. This can result in substantial cost savings, especially if a separate PC/laptop is used for each station (see Figure 3). Consolidation also simplifies management of larger banks of equipment by reducing the number of control points required. Since there are fewer points of potential failure, reliability improves as well.

Supporting multiple protocols through switching can also increase the flexibility of a bridge by enabling it to support multiple interconnects on the output side. For example, by supporting both PCIe and PCI, a bridge can work not only with new PCs and laptops but also older control points that only support PCI. Depending upon the compute capabilities required by the control point, this gives system architects the flexibility to use older equipment that is available for use rather than have to purchase new equipment for this task. In addition, it provides a seamless transition when a PCI-based control point finally fails and needs to be replaced with a PCIe-based platform.

Dual interconnect support can be implemented with a switch and bridge (see Figure 4). The switch controls whether the output port is connected directly to the PCIe output port or through a PCIe-to-PCI bridge. This approach allows additional PCIe endpoints to be connected to a single host controller.

**Signal Integrity**

The issues affecting reliability are vastly different between a low-speed interconnect and one based on high-frequency signals. Even at its highest data rates, an RS-232 interconnect could be run 300 meters without causing reliability concerns. At the higher frequency of PCIe, however, signal integrity becomes more of a concern because of its greatly susceptibility to noise.
For example, if the converter is a standalone box, data will need to run over a combination of a cable, multiple connectors, PCB traces and vias, all of which degrade the PCIe signal. Even with a PCIe plug-in card that does not require a cable, signal integrity can still be an issue, depending upon how far into the PC or laptop the PCIe controller is located, whether low-cost components were used in the signal path and how carefully the traces were laid out.

A clean signal on the receiver side will appear to have what is referred to as an open eye. As signal losses increase, the signal eye will close, as shown in Figure 5a. Performance and reliability of the interconnect will degrade as well. Note that even though the PCIe interconnect may be carrying relatively little data, it is still sending it at 2.5 Gbps, so signal integrity needs to be considered. Most common in embedded platforms today, PCIe 2.0 5 Gb definitely presents a signal-integrity challenge to designers. The typical embedded CPU has limited drive capability, which shortens the PCB trace distances. Compounded with signal path connectors, vias and even trace pitch distances, a redriver or repeater becomes necessary in many platforms.

To open the signal eye and restore signal integrity, a redriver or repeater can be placed in the signal chain. A redriver is a bi-directional signal conditioner that uses equalization and pre-emphasis to compensate for known losses. On the transmit side, the redriver boosts the signal to closely match losses. The signal still experiences losses as it travels to the receiver, but instead of the signal arriving with a closed eye, the signal more closely resembles the original signal (see Figure 5b). Similarly, a redriver can also restore the signal quality of received signals by compensating for known losses along the signal path (see Figure 5c).

Another aspect of signal integrity to consider is the accuracy of the timing source. Because PCIe signal frequency is dependent upon the system clock, any jitter and drift introduced by the clock degrades signal integrity. Utilizing a low-jitter timing source eliminates these concerns and maximizes signal integrity from its source on.

Increasing signal integrity can simplify the design and use of a converter in several ways. First, signals can be sent reliably over greater distances. This means longer, more convenient cables can be used, and the signal can travel over longer PCB traces. On the converter side, this gives developers greater signal margin to work with, either to relax other design constraints or use less-expensive components. Alternatively, the bridge can compensate for potential signal losses in the receiving control point.

Maintaining compatibility of legacy equipment to modern diagnostic equipment enables system architects to continue to maximize utility over the equipment’s operating life. By employing switching, signal conditioning and low-jitter timing technology, OEMs can provide flexibility, efficiency, and reliability while lowering operating costs and easing management complexity.

Rakesh Bhatia is a product marketing director for PCIe products at Pericom and has over 15 years of semiconductor industry experience. Rakesh has published several articles and white papers. He has a B.S. in electrical engineering from University of Houston and an MBA from California State University.
PCI Express (PCIe) is a multi-line, high-speed serial bus interface that can operate at up to 8 gigabits per second per lane of traffic with up to 16 lanes of communication utilized between transmitter and receiver. One lane designates both a differential transmit and receive pair of conductors. PCI Express is owned by a non-profit organization called the PCI Special Interest Group (PCI-SIG) which consists of just under 800 member companies. The PCI-SIG announced last year that the next generation of the standard, PCI Express 4.0, will double the data rate compared to the current generation, achieving 16 gigabits per second. With each new generation, the task involved in validating the electrical performance of an integrated circuit, endpoint (add-in card) or root complex (system) device becomes more complicated.

Faster Data Rates Complicate Testing
When the PCIe standard came on the scene just over 10 years ago it operated at a single speed of 2.5 gigabits per second. Testing this technology was straightforward as a single capture of each lane of the transmitter was all that was needed to perform an analysis of transmitter characteristics such as eye opening, jitter and voltage levels. Now the PCI-SIG has added two additional data rates (5 gigabits/s and 8 gigabits/s) and additional levels of de-emphasis for each of those new speeds. De-emphasis (or pre-emphasis as it is sometimes called in other standards) is a transmitter-oriented type of equalization. The non-transition bits in a transmission sequence are “de-emphasized” electrically such that the change in electrical levels between the transition and non-transition bits compensates somewhat for the inverse of the step response of a given channel. Ideally, the signal amplitude of both transition and non-transition bits should be roughly the same when measured at the end of a channel.

For PCIe 1.0, only one de-emphasis level was used. For PCIe 2.0, two different levels of de-emphasis are specified for the transmitter (-3.5dB and -6dB). Generally, the more de-emphasis at 5 GBit/s, the longer the channel used in the system. PCIe is designed to support two different channel lengths. A short (or client) channel is about 10 inches (25cm) and can have up to one connector. The PCIe standard also supports a longer 20-inch (50cm) channel with two connectors. The shorter channel tends to be more reflection-dominated and the longer channel tends to be more loss-dominated. For PCIe 3.0, each of these channel topologies are also supported; however, at 8 GBit/s, there is a significant amount of loss at the nyquist frequency of 4GHz so that transmitter-based equalization was insufficient to guarantee that a long 20-inch channel would be a stable and interoperable architecture. Thus, for PCIe 3.0 the de-emphasis space was significantly expanded and a receiver equalization requirement was also added. For simplicity, the PCIe 3.0 standard requires a transmitter to drive 11 different de-emphasis levels at 8 GBit/s. These 11 different levels are designated as “presets” and are numbered P0 through P10.

Test Requirements for Current Generations
The testing of all current generations of PCI Express from PCIe 1.0 to PCIe 2.0 to PCIe 3.0 requires testing the output of a transmitter not only at the different supported speeds of 2.5GBit/s, 5GBit/s and 8GBit/s, but it also requires that each de-emphasis level be tested at each supported speed. In the worst-case scenario it is necessary to test 14 different signal conditions for each lane supported by a device. For example, with a 16-lane PCIe 3.0 device it would be necessary to test 14 signals multiplied by 16 lanes which equals a total of 224 signals!

In the case of both add-in cards and motherboards, capturing signals usually involves dedicated PCIe test fixtures (that can be obtained from the PCI-SIG), test cables, adapters and a real-time oscilloscope. The device under test (DUT) is placed in either a compliance load board for testing a root-complex device, or compliance base board for an endpoint device. The PCIe DUT can automatically generate a test signal and can be toggled to each of the three data rates using a specialized function integrated into each standard test fixtures. A typical test session follows these steps:

- PWR up DUT (@2.5GT), capture 250k UI waveform
- Toggle to 5GT/-3.5dB, capture 1M UI waveform
- Toggle to 5GT/-6dB, capture 1M UI waveform
- Toggle to 8GT/s Preset 0 (P0)
- Capture 1.6M UI waveform
- Repeat thru P0 - P10
If the DUT is a 16-lane device, it would be necessary to move cables from lane to lane until all lanes are tested. In addition to 50 ohm terminators must be inserted into each unused lane that is not being tested. As cables are moved from lane to lane, the terminators must also be moved. Since the CLB and CBB fixtures used for PCIe 3.0 testing use small SMP connectors, the small SMP terminators must be carefully removed and reinserted with care to not damage or bend the center pin.

PCI Express 4.0 Will Add Even More Complexity
Keep in mind that PCIe 4.0 is in development and it will add significantly to an already complex and cumbersome test process. At 16 GBit/s, PCIe 4.0 will add another 11 de-emphasis presets, each operating at the new higher rate. This means that a PCIe 4.0 device having 16 lanes will require the testing of 25 signals per lane for a total of 400 test signals that must each be configured, captured and analyzed.

In order to alleviate some of this complexity, it is possible to use high-frequency, high-quality switch networks to perform the task of multiplexing the lanes of a PCIe device into the limited (two or four) channels of a real-time oscilloscope. There are a variety of microwave switch networks available in multiple configurations. These switches can support six differential lanes into a single differential output. There are other switches that can support 16 differential lanes into two differential outputs. Also, multiple switches can be cascaded together in order to expand the capacity of a single switch to support as many lanes as might be desired.

Pros and Cons of High-Frequency Switching
The biggest advantage of using a high-frequency switch as part of the setup for testing a multi-lane PCIe switch significantly decreased test times. It is possible to cut your overall test time by 50% when using a switch network because it is no longer necessary to manually change cable configurations on the test fixture. Other advantages include the elimination of connection errors. Once the setup has been properly configured and verified, it doesn’t have to be touched again so there is no risk of not seating a SMP cable properly into the connector. Test fixtures gain increased service life since you eliminate the multiple insertion/removal cycles and this lowers the risk that a test fixture might be accidentally damaged. Lastly, there is the opportunity to have an automated control program oversee both the tests that are executed and the automatic switching of the lanes being tested. Switches thus offer the promise of significant time savings through programmatic test automation, which can both speed up the completion of tests and increase the quality and consistency of test results from DUT to DUT.

The use of switches does, however, have some disadvantages. For example, even though microwave switches typically have an analog bandwidth of 26 GHz, they still are not completely lossless. Using switches for multi-lane testing also requires multiple cables which add attenuation to the signals being analyzed. And finally, switches are not free. Because they offer a high-quality connection between the DUT and the instrumentation, they can cost $5K-$15K depending on the configuration used.

One way to overcome the additional loss of adding a switch network is to measure the loss of each channel of the switch that you are using along with any additional cables. Once you have measured each channel, it is then possible to apply a filter within the oscilloscope that will compensate for the loss of the switch and the cables and connectors.

![Figure 1: An Agilent U3020A S26 26.5GHz switch to multiplexes multi-lane PCI Express signals into a high-performance real-time oscilloscope.](image1)

![Figure 2: An Agilent E5071C 20GHz ENA Network Analyzer is used to calculate the frequency-dependent performance of the combined cable, SMA adapter and microwave switch network.](image2)

![Figure 3: The Agilent DSO-X 93204A 32GHz oscilloscope supports an optional TDT analysis tool that compares to a VNA-based approach to measuring frequency-dependent characteristics.](image3)

![Figure 4: Using the U3020A switch to measure 5 lanes of PCIe Express 8GT/s signals, this chart shows that using a switch with either VNA- or TDT-based compensation actually measures larger eyes compared to measurements performed without either a switch + compensation.](image4)
There are a number of tools which can be used to measure each signal path through the switch. One way is to measure each path using a vector network analyzer (or VNA). The VNA will capture the frequency-dependent loss characteristics of each signal path, which you can then load into your oscilloscope and, with the appropriate hardware (or software option), create a filter which exactly compensates for the specific loss profile of each signal path through the switch network. As long as the signal path has less than about -10dB of loss at the highest frequency you choose to measure, you should be able to compensate for the switch accurately without also amplifying a significant amount of random noise.

Not all labs have access to a VNA so there are other options for measuring the frequency-dependent loss characteristics of a switch. The Agilent 90000 X-series oscilloscopes for example, have an option called Precision Cable which allows you to characterize switch and cable characteristics up to about 36GHz using an approach similar to a TDT. Likewise, if you have access to a TDR, you can also use it to measure the frequency-domain performance of the switch and cable paths.

In Figure 4, you can see two different approaches to using frequency-domain analysis of signal-loss characteristics to compensate for cable and switch losses. What is interesting is that eye-height measurements for an 8GBit/s signal through a compensated switch were about 15-20% larger compared with using a simple, direct-cabled connection (no switch) to the DUT.

In conclusion, switching is the only way to greatly simplify the testing of multi-speed, multi-lane serial busses by eliminating the need to change connections. Nevertheless, using switches in a test setup also demands the use of signal-path measurement and tools and techniques to compensate for the additional loss resulting from the use of the switch and additional cables. Using the right equipment, switches can not only speed up your measurements but can also give you results that compare favorably or even exceed current test practices.
Modern Technology in a Traditional Form Factor

New products combine the advantages of modern processor and interconnect technology such as PCI Express with the benefits of the traditional VME form factor.

By Ákos Csilling, CES - Creative Electronic Systems SA

Traditional VME form factors are more and more relegated to legacy status, with most new high-end systems being implemented in VPX. Yet not all applications require huge bandwidths or a large number of high-speed connections. In many cases the previous investment in the enclosures and custom boards fully justifies the choice to stick to the VME format. On the other hand, the traditional VME and PCI buses are often unable to meet the current data transfer requirements. In addition, the industry-standard single-board computers often rely on single-source interface components, which may also present obsolescence issues.

Many avionic computers require multiple avionic interfaces, some video or signal processing capability and onboard data storage. These types of computers provide important, but not critical functions (Design Assurance Level DAL-C or D per FAA guidelines). The console and Ethernet interfaces are often used for maintenance and non-critical communication. The entire system must be rugged to resist the environmental conditions of the aircraft, with extreme temperatures, vibration, EMI/EMC and various contaminants.

In the past, this would require multiple single-board computers in VME or CPCI format, each providing a subset of the functions. The limited interconnect bandwidth would limit the performance and require careful partitioning of the application in order to limit the data-exchange requirements. Time synchronization among the SBCs would be critical, in order to ensure coherent operation of the various interfaces.

Today, a single processor, possibly with multiple cores, can do the job. One core can be dedicated to time-critical functions, while the other can offload non-critical activity. On the other hand, the connection to the multiple I/O interfaces requires more bandwidth than a traditional VME or PCI bus. PCI Express can provide this additional bandwidth in a simple and software-compatible way. PCIe is readily available in modern processors and FPGA devices. A single Gen 1.0 PCIe x4 interface can transfer 2 GB/s. Most functions are available as XMC modules that can be directly plugged onto the SBC, or onto a suitable carrier.

Figure 1: Block diagram of a typical avionic computer platform. A single modern CPU, with an FPGA for simple I/O customization, extended with a solid-state storage device, a PMC or XMC for avionic interfaces and a video-processing mezzanine.
The VITA 41 (VXS) format replaces the VME-P0 connector with a more powerful one that allows the transmission of eight pairs of high-speed signals, up to 10Gb/s; for example PCIe, SRIO or any other serial protocol. The standard allows the signals to be routed in multiple topologies, for example in a daisy chain to adjacent slots, or in a star or dual-star to one or two central switch slots, for larger systems. While VXS does definitely increase the bandwidth available, and does allow the coexistence of new and old boards, it also requires a new backplane. Still, VXS is successful in a number of applications where it allows a gradual transition from VME or CPCI to a switched serial fabric.

The PCIe over P0 technology introduced recently by some vendors extends this possibility to the traditional VME form factor. This new technology allows the continued use of the existing VME64x systems, including the backplanes and legacy boards, to achieve up to 2 GB/s point-to-point transfer rates. The technology is based on a special P0 connector on the board in order to provide extended signal integrity to allow the establishment of PCIe links between two or three VME slots over the traditional VME-P0 connector of the backplane. These signals are not routed in the backplane, but in a custom overlay, allowing any interconnect topology. This technology provides a cost-effective solution to increase data transfer rates between a small number of processors in any VME64x systems, without the need to replace the existing backplane.

Recently, for the design of a new flight computer with multiple avionic interfaces including discrete signals and serial ports, input video channels and onboard data storage, CES decided to use a traditional VME format. The RIO6-8096 was chosen as the main processing element, with a storage XMC installed directly on this SBC. The optional FPGA on the RIO6 was used to provide discrete and serial I/O. The electrical interfaces for these signals were installed on an overlay backplane, which also provided the PCIe link through the VME-P0 to a switching carrier installed in a second VME slot. An avionic I/O module and a video compression engine were installed on this carrier, completing the functionality.

A sealed, conduction-cooled enclosure was already available, with an integrated VME64x backplane and power supply. The external connectors and the electrical protection devices were installed on a separate protection board, linked to the overlay backplane through a flexible PCB connection, with an additional board for the electrical filter and the hold-up capacitors.

The resulting design provides new technology with the Freescale QorIQ processor and the PCIe interconnect in the proven mechanical and electrical environment of a VME64x system.

Ákos Csilling is a product development manager at CES - Creative Electronic Systems SA. He works with the CTO on the product strategy and roadmap. Previously he managed the development of VME-based and custom avionic computer platforms. Before he joined CES in 2003, he was a post-doctoral fellow at CERN, the European Organization for Nuclear Research. He holds an MSc and a PhD in Physics from Eotvos University in Budapest and is pursuing an executive MBA at HEC Geneva.
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Accelerate Server-based Media Processing

A PCI Express media processing accelerator card using DSP technology offers benefits over additional servers for high-density voice and video processing in network applications.

By Brian Carr, Emerson Network Power

“These go to eleven,” were the legendary words of Spinal Tap lead guitarist Nigel Tufnel when explaining why the band’s amplifiers made them louder, and therefore better, than other rock bands. The expression now has its own entry in the Oxford English Dictionary and has come to mean the act of taking something to the extreme. When talking about communications networks, taking the performance of an application to eleven usually means adding more equipment. This is especially true when adding functionality without compromising performance of the original applications on equipment such as rack mounted servers and appliances.

For example, high-density voice and video processing is increasingly in demand for network applications and the current typical solution is some kind of commercial host media processing (HMP) solution that draws on the existing processor resources of the server.

This article describes an alternative approach, using PCI Express media acceleration cards—which are increasingly available off the shelf—and embedded voice/video firmware to offer dramatically improved performance while taking up less space, consuming less power and costing less. In short, a solution that can take a server-based media processing application to eleven.

As communications networks transition to an all-IP environment, service providers and network operators are finding a need for IP media servers and new advanced flow management devices such as session border controllers, QoS analytic engines and intelligent flow optimizers.

Many of these are developed and deployed on 1U or 2U standard rack-mounted server architectures for simplicity. The role of IP media gateways and media servers is clear but as the developers and users of border flow management devices consider where to go next, one obvious step is to build some advanced media stream processing into the platform. One key concern is scalability. According to most analysts, mobile data and especially mobile video is expected to grow exponentially over the next three to five years so the pressure is on to find cost and power-efficient ways to scale media processing to suit. Some of the issues that confront equipment developers are as follows:

Adding Voice Transcoding to a Session Border Controller

A good example of a flow management application is the session border controller (SBC), an often-quoted example of a class of equipment known as network security gateways. These are characteristic of “bump in the wire” devices that form a bridge between trusted and untrusted networks or enterprises. Their job is to analyze and characterize incoming IP traffic, block undesirable or unauthorized flows and let through approved traffic. In communications networks, a lot of this traffic is media streams.

As this is a gateway point, many SBC users are also interested in providing additional media format translation in addition to the stream management. Even simple requirements like DTMF tone monitoring require that the media streams are decoded and analyzed.

The ability to have voice transcoding within the box helps simplify the communications flow for an operator, hence provides a competitive advantage for the equipment vendor. Unfortunately, voice and especially video stream processing...
in real time at high channel counts is a strenuous task, so adding this function can impose a significant reduction on the processing power available to the main service leading to a reduction in capacity.

Possible Solutions
Adding media processing functionality to an application can be done in a number of ways:

• An additional system or device linked to the original appliance
• An internal software solution, adding functionality to existing software
• An internal media processing accelerator offering hardware-accelerated transcoding

In the SBC plus voice transcoding example above, using an external media gateway is perhaps the simplest to envisage. The border gateway terminates principal traffic streams, and redirects media to the external gateway for transcode via external ports. Media can come back into the border gateway for egress filtering. The disadvantage is that this is costly, uses rack space and extra power, takes up valuable physical network interfaces off the border gateway, and still requires application development that controls and configures media stream handling on a stream by stream basis.

Taking the media server plus HD video example above, using an external HD conferencing device will be complex to manage, will take up additional rack space and power, and could be high cost. The service application would need to be able to manage both systems in parallel, potentially increasing complexity, management overhead, and OPEX costs. Upgrade paths to newer compression schemes such as H.265 may be limited.

The other two solutions allow for this function to be taken inside the box.

An internal software solution, for instance using commercially available host media processing software, necessarily makes use of internal processing resources.

In the case of voice transcoding, this may be a great solution for a moderate number of simultaneous channels, however it does not scale effectively. At upwards of 1200 simultaneous channels of G.729 encoding, the software solution approaches 50% utilization of a typical server, starving the original application of processing resource. Effectively this means that additional servers would be required to offer higher densities of voice transcoding, and the cost of the commercial software that is usually charged on a per-channel basis soon mounts up.

Although it is possible to add more servers to address this issue, accepting a reduction in capacity even for an improvement in functionality is often difficult to manage from a product line perspective. It results in a downgrade of capacity within the same product offering, so cannot really be viewed as adding functionality. Matters get even worse when considering field upgrades since a customer must accept that a given installation would no longer be able to carry the same traffic.

The Solution
A more elegant solution to the problem is to use a plug-in media processing accelerator to offload both audio and video processing from the server host.

This keeps the function internal to the network element AND avoids the loss of central processing resource that would otherwise be required to run a fully software solution. Ideally this would be able to take account of new voice and video compression schemes as they emerge. In this case, using a plug-in media processing accelerator offers a true upgrade path.

DSP Offload Card
It is now possible to deploy PCI Express media processing boards that offer high-performance voice and video transcoding based on digital signal processing (DSP) technology. Some boards even offer voice and video processing firmware optimized for their DSP array. Application developers can interact with these boards via a simple object-oriented application programmers interface (API). The transcoding performance scales linearly according to the number of DSPs that are fitted—options from 4 DSPs to 12 DSPs are available. But even with 4 DSPs and consuming less than 25W of power, cards are available that deliver a voice transcoding performance comparable to a typical server consuming 300W or more.
An Example Application
An example may help illustrate the value of using acceleration. Consider a packet processing application that, in a server based on dual Intel® Xeon® processors, can support 4000 concurrent sessions or streams. The market now demands to add voice transcoding capability.

As outlined above, one option is to use a commercial host media processing solution. This requires approximately 50% of a dual Intel Xeon server capacity for 2000 transcode streams. As a consequence, adding this capability reduces the available processing power for the original application by 50%. The resulting solution is now only a 2000 stream processing device. To get back to the 4000 stream capacity, a customer must buy two units, so power consumption and rack space is doubled.

The alternative is to add a PCI Express media accelerator card. This takes care of the processing-intensive workload, thus maintaining the original performance. In fact, compared to a host media processing solution that is limited to approximately 2000 sessions per server, a single PCI Express media accelerator card may be capable of transcoding over 7500 bidirectional voice streams or over 300 mobile video streams in hardware, and multiple boards can be fitted to a single server.

Voice Capability
When considering the PCI Express accelerator card route, design engineers should ensure their shortlisted solutions support the following 3GPP, ITU-T, IETF and other voice codecs:

- Uncompressed telephony: G.711 μ-law/A-law with Appendices I and II
- Narrowband compression: G.729AB, G.729.1, G.723.1A, G.726, G.727
- Wideband compression: G.722, G.722.1
- Wireless network: GSM EFR, AMR and AMR-Wideband; EVRC and EVRC-B
- Internet voice: iLBC, SILK (Skype), Opus [roadmap]

In addition, each voice channel should support echo cancellation, announcements, conferencing, mixing, and a full range of tone detection and relay functions.

Video Capability
HD (or other) video streams can be redirected within an appliance to a PCI Express accelerator card and transcoding and conferencing can happen without making any use of existing processing resource. For example, some PCI Express media accelerator cards can handle up to six 4-party video conference bridges where each participant uses H.264 720p at 30fps. There are also cards that can handle resizing to and from 1080p.

Design engineers should ensure the solution they choose supports the most common video compression schemes used in communications, such as H.263 (legacy) and MPEG-4 for CIF, and H.264 at resolutions up to 1080, and is easily upgradeable as newer compression schemes emerge.

Many rack mount servers are available in fully NEBS compliant, hardened versions, so the accelerator card should be designed for NEBS carrier grade and data center environments, so offering a common solution for both enterprise and telecom environments.

A Better Solution
High density voice and video processing is increasingly in demand for applications such as session border controllers, media gateways/servers or media resource functions, video or content optimization, video communications servers, and interactive voice and video response systems. We can see that using a PCI Express media processing accelerator card rather than additional servers has a lot of benefits:

- It takes up less space
- It consumes much less power
- It can easily be retro-fitted to existing deployed systems as a true feature addition
- It costs less than a comparable server + commercial host media processing combination for the same performance

Consequently, it offers a lower total cost of ownership and a much simpler upgrade and deployment experience. In the words of Spinal Tap’s Nigel, “They go to eleven. They’re one better.”

Brian Carr is strategic marketing manager for the Embedded Computing business of Emerson Network Power, with a particular focus on communications markets and applications including wireless, wireline and service delivery. A widely published author and accomplished speaker on AdvancedTCA technology and applications, Carr has also represented Emerson on conference advisory boards and industry consortia. He holds master’s degrees in engineering from Cambridge University and in information technology from Essex University.
PCI-SIG-nificant Changes
Brewing in Mobile and Small Form Factor Designs

Of five significant PCI Express announcements made at the PCI-SIG Developers Conference, two are aimed at mobile embedded. It’s about time.

By Chris A. Ciufo, Editor-in-Chief

The big news from the PCI-SIG is speed. From PCI to PCI Express to Gen3 speeds, the PCI-SIG is an industry consortium that lets no grass grow for long. As the embedded, enterprise and server industries roll out PCIe Gen3 and 40G/100G Ethernet, the PCI-SIG and its key constituents like Cadence, Synopsis, LeCroy and others are readying for another speed doubling to 16 GT/s (giga transfers/second) by 2015.

The PCIe 4.0 next step would likely become known as “Gen4" and it evolves bandwidth to 16Gb/s or a whopping 64 GB/s (big “B”) total lane bandwidth in x16 width. The PCIe 4.0 Rev 0.5 specification will be available Q1 2014 with Rev 0.9 targeted for Q1 2015.

Yet as “SIG-nificant” as this Gen4 announcement is, PCI-SIG president Al Yanes said it’s only one of five major news items.

Five PCI-SIG announcements at Developers’ Conference, June 2013

The other announcements include: a PCIe 3.1 specification that consolidates a series of ECNs in the areas of power, performance and functionality; PCIe Outside the Box which uses a 1 - 3 meter “really cheap” copper cable called PCIe OCuLink with an 8G bit rate; plus two embedded and mobile announcements that I’m particularly enthused about. See Table 1 for a snapshot.

New M.2 Specification
One of two announcements for the mobile and embedded spaces, the new M.2 specification is a small, embedded form factor designed to replace the previous “Mini PCI” in Mini Card and Half Mini Card sizes (Figure 1). The newer, as-yet-publicly-unreleased M.2 card specification will detail a board that’s smaller in size and volume, but is intended to provide scalable PCIe performance to allow designers to tune SWaP and I/O requirements. PCI-SIG marketing workgroup chair Ramin Neshati told me that M.2 is part of the PCI-SIG’s deliberate focus on mobile in a fundamentally changing market.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI Express 3.1</td>
<td>Combines engineering change orders into new 3.1 spec for protocol extensions, L1 power substates, lightweight notification, enhanced downstream port containment, precision time measurement, more.</td>
</tr>
<tr>
<td>PCI Express 4.0</td>
<td>Doubles bandwidth to 16 GT/s, 16 Gbps link, and about 64 GB/s total bandwidth (x16).</td>
</tr>
<tr>
<td>PCIe Outside the Box</td>
<td>Cheap, 1-3 meter “really cheap” copper cable starts at 8G bit rate with up to 32 Gbps each direction (x4). Think of it as eSATA for PCIe and used for internal/external storage. Will be “orders of magnitude cheaper” than Thunderbolt, says PCI-SIG spokesman.</td>
</tr>
<tr>
<td>M.2 specification</td>
<td>Replaces PCI Mini cards and designed for I/O modules in ultrabooks, tables, and possibly smartphones. Scalable PCIe I/F.</td>
</tr>
<tr>
<td>M-PCIe</td>
<td>Mobile PCIe uses MIPI M-PHY in a smartphone to connect host ASSP to modem, WLAN, and possibly onboard mass storage.</td>
</tr>
</tbody>
</table>
Mobile PCIe (M-PCIe)

The momentum in mobile and interest in a PCIe on-board interconnect lead the PCI-SIG to work with the MIPI Alliance and create Mobile PCI Express: M-PCIe. The specification is now available to PCI-SIG members and creates an “adapted PCIe architecture” bridge between regular PCIe and MIPI M-PHY (Figure 2).

Using the MIPI M-PHY physical layer allows smartphone and mobile designers to stick with one consistent user interface across multiple platforms, including already-existing OS drivers. PCIe support is “baked into Windows, iOS, Android and others,” says PCI-SIG’s Neshati. PCI Express also has a major advantage when it comes to interoperability testing, which runs from the protocol stack all the way down to the electrical interfaces. Taken collectively, PCIe brings huge functionality and compliance benefits to the mobile space.

M-PCIe supports MIPI’s Gear 1 (1.25-1.45 Gbps), Gear 2 (2.5-2.9 Gbps) and Gear 3 (5.0-5.8 Gbps) speeds. As well, the M-PCIe spec provides power optimization for short channel mobile platforms, primarily aimed at WWAN front end radios, modem IP blocks, and possibly replacing MIPI’s own universal file storage UFS mass storage interface (administered by JEDEC) as depicted in Figure 3.

PCI Express Ready for More

More information on these five announcements will be rolling out soon. But it’s clear that the PCI-SIG sees mobile and embedded as the next target areas for PCI Express in the post-PC era. Yet the organization is wisely not abandoning the PCI Express standard’s bread and butter in high-end/high-performance servers and systems.

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Multiple Processors in High-Performance Embedded Computing: “Only Connect”

Multiprocessing is at the heart of high-performance embedded computing in mil/aero systems—and new technologies enable it to deliver significantly improved performance.

By Peter Thompson, GE Intelligent Platforms

Today’s mil/aero systems are decidedly in the world of multicore processing. Mainstream processors are available with 10 and 12 cores. Slightly more exotic architectures are available with tens to hundreds of cores (Xeon Phi, Tile, GPGPU). This allows abundant processing power to be applied to problems, but how to keep the cores fed with data? An idle core is a wasted resource. It’s not just bandwidth between resources that is of concern—it’s also the latency incurred in transfers. That can significantly affect the bandwidth for small transfers and can also make the system-transfer function exceed its design requirements for real-time operation. Newer architectures allow for techniques such as remote direct memory access (RDMA) and methods that build upon it such as GPUDirect to be employed to address these issues and to build systems that balance data movement with processing power.

The underlying premise of high-performance embedded computing (HPEC) is to leverage the architectures and software that are prevalent in the world of commercial supercomputing and to apply them to the harsh world of mil/aero applications. This has led to a widespread adoption of processors from Intel, AMD and NVIDIA and standard interconnects such as PCI Express, Ethernet and InfiniBand. However, vanilla implementations can fall short of expectations for performance in these demanding applications. For instance, running a TCP/IP stack for a 10GbE link can easily burn up an entire processor core with no cycles left over for computation workloads. Similarly, the measured performance can fall far short of theoretical wire-speed maximums.

Sensor to Processor

On the sensor side, it is common to see FPGAs right behind the analog-to-digital converters, with some kind of data link to the processing system. While it is possible to program FPGAs to talk to most of the major protocols, it is most common to see either PCI Express (which is hard-coded into many devices) or a simple interface such as serial FPDP. In systems where the analog acquisition is co-located with the processing, PCI Express is a common choice, but can suffer from excessive latency and multiple transfers unless some key techniques are employed.

For example, a couple of years ago it was not uncommon to see the data undergo three transfers to get from the sensor to GPU memory ready for processing. This translates into larger latency than may be desired, and to reduced overall bandwidth due to the data being moved three times. This
may be tolerable for some applications (such as synthetic aperture radar, where the acquisition of a complete data set takes a long time, and the calculation of an image is not generally needed immediately), but not for others such as tactical radars and electronic warfare systems where a signal must be received, processed and sent out in as little time as possible.

The solution to this problem lies in technology termed GPUDirect RDMA. The first iteration of GPUDirect removed the host memory-to-host memory transfer by allowing a common address space, eliminating one whole transfer. This reduced latency by around one third. With the introduction of the Kepler family of GPUs and the latest version of CUDA (5.x), NVIDIA removed another transfer step, and now allows the PCI Express endpoint and the GPU to see a piece of each other’s memory, allowing either device to transfer directly to or from the other. This not only removes the need for an extraneous transfer, but also removes the host processor and operating system from the chain. Measurements have shown this to reduce latency by a factor of 15, opening up new application areas for GPGPU. It is worth noting that none of this requires proprietary mechanisms. The interface is standard PCI Express; the transfers use regular DMA mechanisms. It just happens to be that the destination address is an aperture into GPU memory that has been mapped to PCI Express space and is exposed via a simple API call.

Processor to Processor
When it comes to communicating between processors in a multiprocessor system, there are many choices. Intel devices may be connected with QuickPath Interconnect in a symmetrical multi-processing architecture that makes two processors appear to the operating system as a single large CPU. However, this functionality is generally not available in the devices that are provided in the BGA packages from the extended lifecycle portfolios that are favored for rugged environments—only in socketed versions that are not fully rugged or must go through a complex rework process.

Between boards, most of the major fabric choices are available, but the right choice can have a marked effect on system performance. For example, if standard TCP sockets over 10GbE are used, substantial CPU resources are used up just to manage the transfers—and the data rates achieved are less than optimal. If, however, remote direct memory access (RDMA) is available, the picture changes dramatically. RDMA allows the network interface chips to move data directly from the application space on one board to that on another with no extra copies and no involvement of the host processor once the transfer has been requested. This reduces the amount of CPU cycles used to manage the transfer to single digit percentages rather than close to one hundred percent. Examples are RDMA over Converged Ethernet (RoCE) from Mellanox and Internet Wide Area RDMA Protocol (iWARP) from Intel. Both have low latency (as low as 1.3 microseconds for RoCE, 3 microseconds for iWARP). Mellanox also supports RDMA over InfiniBand (using the same network interface controllers (NICs)), allowing the system designer to choose between the two fabrics. The API to the application remains the same thanks to the OFED (Open Fabrics Enterprise Distribution: open source software for RDMA and kernel bypass applications) stack. (Figure 1, Figure 2).

GPU to GPU
Similar data movement issues arise in a heterogeneous HPEC system comprised of one or more host processors and multiple GPUs. In such a system, it is common to view the GPUs as the primary data consumers, with the host processor(s) being relegated to doing housekeeping functions. Once the data has been deposited into a GPU from a sensor interface (using GPUDirect RDMA), after a first stage of processing it may be necessary to move it to another GPU for the next stage of a pipelined processing scheme.
In the past, this would require the data to be moved from GPU memory to its host system memory, then perhaps to another host processor, then finally down to the memory of the destination GPU. Again, multiple transfers, extra latency, wasted bandwidth and unwanted burden on the hosts. And again, GPUDirect RDMA comes to the rescue via two forms of support. Firstly, if the source and destination GPUs reside in the same PCI Express domain, an RDMA transfer is available from GPU memory to GPU memory across PCI Express. This can occur whether the GPUs are both connected directly to the same host root complex, or if they are both downstream of a PCI Express switch—although the latter scenario can lead to better performance.

What if the GPUs are not in the same PCI Express domain? For example, consider two GE Intelligent Platforms IPN251s in a system. (Figure 3, Figure 4). Each IPN251 has a 3rd Generation Intel i7 CPU connected to a 384-core Kepler GPU via 16 lanes of Gen3 PCI Express. Each CPU/GPU cluster also has a Mellanox ConnectX-3 NIC providing two channels of 10GbE and/or DDR InfiniBand for inter-board communication. By leveraging another form of GPUDirect RDMA, it is possible now for one GPU to RDMA data to a remote GPU across PCI Express (from GPU to NIC) and InfiniBand (from NIC to NIC—most likely via a system level switch). Again, this avoids multiple transfers and does not require host intervention.

**CPU to GPU**

These transfers have always allowed for DMA across the PCI Express bus between system and GPU memory, generally relying on a DMA engine built into the GPU.

**The complete system**

By combining these mechanisms, it is now possible to construct an HPEC system for processing sensor data for a variety of mil/aero applications including radar, electronic warfare, synthetic vision and many others that not only optimizes processing power by mixing FPGAs, general-purpose processors and GPUs, but also optimizes system data flow to minimize latency, maximize bandwidth utilization, and maximize processor utilization for computation rather than data movement.

**Open architecture software**

While the low-level implementations of these transfer mechanisms may use proprietary APIs, in many cases it is possible to use them via high level open-standard APIs. Now, portable OSA applications can leverage the performance boosts of RDMA without having any hardware-specific ties. For example, the message passing interface (MPI) library can be layered over OFED, allowing applications using this commonly used API to take advantage of RDMA transfers between processors without any hardware-specific code. Similarly, MPI transfer primitives can copy data directly between CPU and GPU memory. An optimized MPI library can differentiate between device memory and host memory without any hints from the programmer and can use the appropriate RDMA transfers.

The different RDMA methods described (sensor to GPU, CPU to GPU, CPU to GPU, GPU to GPU) are frequently employed at the same time in a system to optimize end-to-end data movement. The result can be a huge increase in performance of the system, allowing reductions in SWaP, increased functionality, or enabling applications that were previously not a good fit for such programmable, scalable architectures.

Peter Thompson is senior business development manager, High Performance Embedded Computing at GE Intelligent Platforms. With an honors degree in electrical and electronic engineering from the UK’s University of Birmingham, Peter has worked for over 30 years in embedded computing. defense.ge-ip.com.Trillium, and ObjectStream. Drew has a BA in human services from Western Washington University in Bellingham, WA.
USB 3.0 is ubiquitous in new PCs as a standard feature, but it’s commonly considered to have come later to the market than consumers would have preferred. Anyone who purchased a new Apple iPod and had to endure the transfer 10+ GB of data over a USB 2.0 connection would have preferred USB 3.0 speeds. Digital cameras take and store pictures that are 3 MB per image and more. Digital video cameras record video at the rate of about 10 minutes per gigabyte. HD video recorders use a "raw" file format that records even more detail in an uncompressed format, which creates noticeably larger files. So while USB 3.0 is ubiquitous and popular in new PCs, it would have been just as needed and popular three years ago. While we could ponder on the question, “Why is USB 3.0 so late to the market?” it’s more informative for us to consider what consumers will need in 3 years.

**Trends in Storage and Prices**

The capacity of hard disk drives (HDDs) and solid state drives (SSDs) continues to increase, and prices per gigabyte to decrease. While HDDs will be the common way to store huge amounts of data, the price of SSDs will drop more quickly. The prevalence of “instant on” smartphones and tablets, which take advantage of SSD performance, has made consumers want the same from their laptops. SSDs also have the advantage of consuming less power which extends battery life. Basically, consumers are used to the performance and battery life offered by their devices using SSD, and this will drive even greater demand for SSDs over HDDs.

In addition to “instant on” performance and low power consumption, the price of SSDs is consistently going down, even with increasing performance. Today, a 256 GB SSD from Crucial or Sandisk sells for about USD$170 retail. This SSD can read data at 5.4 Gbps and write data at 4.4 Gbps using SATA 6 Gbps interfaces, which are faster than the effective USB 3.0 throughput rates of 3.2 to 3.5 Gbps. Assuming prices drop by about 50 percent each year (as has been the trend so far), the retail price of a 256 GB SSD will drop to $21 within 3 years (Figure 1). We can assume a retail margin of 30 percent for the retailer (not the flash memory maker), so the estimated cost of this memory to the SSD maker is $120.

And so, if the cost to the manufacturer is about $120 today, the cost for that same memory will drop 50 percent a year to about $15 by 2016. Even if the drop is only 30 percent a year, the cost drops to about $29. Either way, the integration of this much memory is highly compelling to consumer device manufacturers of cameras, smartphones, tablets, and “phablets” (i.e., smartphones with almost tablet-sized screens).

Using a similar extrapolation which assumes the doubling of memory capacities each year at the same price point, $170 will buy a 2 TB SSD in 2016 (Figure 2).

Looking at this trend, tablet and smartphone designers are making the obvious choice to increase their products’ storage capacity. More importantly, system architects in a wide variety of consumer industries are integrating SSDs into their products while increasing their products’ appeal by integrating higher-quality digital video cameras and digital cameras. Larger files, from photos and videos, in greater capacities of high-performance memory, leads to consumer
demand to move the data more quickly. So begins the battle of the standards.

**Competing Standards**

In 2012, Apple launched monitors and PCs with the Thunderbolt standard, which supports 10 Gbps transfer speeds. As usual, Apple is ahead of everyone else. Thunderbolt supports video and data multiplexed through a single cable. MacBook Air or Pro PCs can be connected to either an Apple monitor or a Thunderbolt docking station. The same Thunderbolt cable carries a multiplexed 10 Gbps PCI Express (PCIe) connection that can carry data from the MacBook to the monitor and other devices plugged into the monitor or docking station. In addition, the PCIe connection allows the docking station or monitor to integrate a USB 3.0 host to connect to USB peripherals and/or Thunderbolt devices like HDDs. In this case, the USB 3.0 host is in the docking station, not inside the PC.

Apple uses Thunderbolt to fill its customers’ need for a fast external interface. In fact, the next generation of Thunderbolt will go to 20 Gbps to carry 4K video to meet the demand for a faster interface. The problem is that Thunderbolt is a closed standard. It requires discrete chips in both the host and client. It requires an active cable with chips embedded in the cable. Adding Thunderbolt increases a system’s cost by $10-25.

On the other hand, integrating USB 3.0 has a much lower price point. In fact, every major PC manufacturer currently produces a USB 3.0 docking station based on a DisplayLink chip. The docking stations allow consumers to use existing USB 3.0 drivers concurrently with existing USB 2.0 and 3.0 peripherals. One USB 3.0 cable connected to a USB 3.0 docking station can support multiple USB 1.1, 2.0, and 3.0 peripherals, in addition to HDMI monitors. ASUS, HP, Fujitsu, Toshiba, Lenovo, and Dell built docking stations based on USB 3.0 to provide the same functions as Thunderbolt. The enhanced SuperSpeed USB 3.0 specification will provide the same ease-of-use and functionality, but at the increased speed of 10 Gbps.

This brings us back to the most compelling use of the smartphones, tablets, and phablets: These mobile devices already can edit videos, play games, and manipulate spreadsheets. Using standard USB drivers, consumers can use mobile devices with their existing USB 3.0 docking stations to make the mobile devices their primary computing platform. The docking station lets them use a full-size keyboard, mouse, 30-inch monitor, and 3 TB SSD drive, effectively removing the limitations of a tiny screen. As mobile devices become more powerful and include larger embedded SSDs, using 10 Gbps USB 3.0 in a single, small form factor connector becomes even more compelling to both low-end and high-end mobile devices.

**Open-Standard 10 Gbps SuperSpeed USB 3.0**

The new 10 Gbps SuperSpeed USB 3.0 specification will run at 10G, which matches Thunderbolt’s stated performance. 10 Gbps SuperSpeed USB 3.0 will use the same legacy connectors as the original USB 3.0 as well as the same driver software. As an open standard, PC and consumer product makers can easily adapt to it. The USB-IF will continue its successful process of rolling out widespread, solid specifications (as it has with USB 1.1, 2.0, and 3.0) by working with multiple industry leaders for their technical input. They will back the new specification with a strong testing and certification process to ensure interoperability. Most importantly, consumers recognize USB as the interface on their phones, tablets, TVs, and cameras. 10 Gbps SuperSpeed USB 3.0 will be the standard consumers need just as they realize they need it.

Eric Huang worked on USB at the beginning in 1995 with the world’s first BIOS that supported USB keyboards and mice while at Award Software. After a departure into embedded systems software for real-time operating systems, Eric returned to USB cores and software at inSilicon, the leading supplier of USB IP in the world. inSilicon was acquired by Synopsys in 2002. Eric served as Chairman of the USB On-The-Go Working Group for the USB Implementers Forum from 2004-2006.

Eric Huang received an M.B.A. from Santa Clara University and an M.S. in engineering from University of California Irvine, and a B.S. in engineering from the University of Minnesota. He is a licensed Professional Engineer in Civil Engineering in the State of California.
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FEATURES & BENEFITS

◆ Digital Input / Output PCI Express DAQ Products for compact control and monitoring applications. Choose from 8 to 120 channels offering various voltage, isolation, speed, and counter/timer options.

◆ Serial Communication PCI Express Products. Designed for use in retail, hospitality, automation, games, as well as point of sale systems and kiosks.

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TECHNICAL SPECS

◆ Serial COM cards feature 2, 4, and 8-port versions with 128-byte FIFOs for each TX and RX. Software selectable RS-232, RS-422, and RS-485, per port and custom baud rates.

◆ Isolated PCI Express RS-232/422/485 cards feature speeds up to 3Mbps and 2kV isolation port to port and port to computer on all signals.

◆ PCI Express digital cards feature Change of State (COS) detection and interrupt capabilities, optional 82C54 Counter / Timers, and 3.3V LVTTL signaling.

◆ PCI Express isolated digital input and relay output cards are available in 4, 8, or 16-channel versions and are optically isolated channel to channel and channel to ground.

APPLICATION AREAS


AVAILABILITY

Now

CONTACT INFORMATION

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FEATURES & BENEFITS

◆ Precision 16-Bit analog outputs: DAC per Channel
◆ 256K-Sample output data FIFO buffer; Configurable as open or closed (circular)
◆ High accuracy ensured by on-demand Autocalibration of all channels, with outputs forced to zero during autocalibration.
◆ Multiboard synchronization supported
◆ Output clocking rates to 500K samples per second per channel with all channels active

TECHNICAL SPECS

◆ +3.3VDC ±0.2 VDC from the PCIe bus, 0.9 Amps typical, 1.0 Amps maximum.
◆ +12VDC ±0.4 VDC from the PCIe bus, 0.5 Amps typical, 0.6 Amps maximum.
◆ Total power consumption: 9.4 Watts typical, 11 Watts maximum. All outputs loaded with 1.0mA

APPLICATION AREAS

Precision Voltage Array Servo Control Waveform Synthesis High Density Outputs Process Control Industrial Robotics

AVAILABILITY

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PLX Technology

ExpressLane™
PCI Express 3.0/2.0/1.x

OS Support: Windows, Linux, Others
Bus Interface: PCIe

PLX Technology (NASDAQ: PLXT), a leading global supplier of software-enriched silicon connectivity solutions for the enterprise and consumer markets, offers the industry’s broadest portfolio of PCI Express Switches and Bridges. With a rich history of leadership in PCIe, PLX has been first to market across all families and carries the lowest power, lowest latency, and unmatched feature-set of any supplier.

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FEATURES & BENEFITS

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◆ ExpressLane PCI Express Bridges provide forward and reverse bridging. Our PCIe Bridge family allows designers to migrate local bus, PCI and PCI-X bus interfaces to the serial, PCIe Architecture

AVAILABILITY

All products shipping today

APPLICATION AREAS

Data Center and Cloud Computing, Graphics, Industrial, Embedded, Consumer

CONTACT INFORMATION

PLX Technology, Inc
870 W. Maude Ave
Sunnyvale, CA 94085
USA
plxtech.com
ExpressLane™
PCI Express 3.0 Switches

OS Support: Windows, Linux, Others
Bus Interface: PCIe

The new innovative PLX® ExpressLane™ PCIe Gen 3 switch family, designed on 40nm process node, includes broad lane counts ranging from 12 up to 96 lanes. Board and system designers can take full advantage of the latest PCIe specification—8 Gbps in both directions (Tx/Rx), per lane—thus enabling one PLX 48-lane Gen 3 switch to handle an astounding 96 Gbps of full peer-to-peer bandwidth. PLX’s Gen3 switches also offer hot-plug controllers, virtual channels, virtual channels, multi-root functionality, and integrated DMA.

PLX PCIe Gen 3 switches include exclusive software driven on-chip hardware debug and monitoring features such as measurement of the SerDes eye inside the device; PCIe packet generation to saturate x16 Gen 3 port; injection of error in live traffic; error logging; port utilization count; as well as PCIe and traffic monitoring for easy bring-up of PCIe systems that would otherwise require days of lab set-up and hundreds of thousands of dollars in test and measurement equipment. Furthermore, PLX offers designers a software development kit that simplifies design-in of the switch and its value-added features.

FEATURES & BENEFITS

◆ PEX 8796: 96 lanes, 24 ports
◆ PEX 8780: 80 lanes, 20 ports
◆ PEX 8764: 64 lanes, 16 ports
◆ PEX 8750: 48 lanes, 12 ports
◆ PEX 8749: 48 lanes, 18 ports
◆ PEX 8748: 48 lanes, 12 ports
◆ PEX 8747: 48 lanes, 5 ports
◆ PEX 8734: 32 lanes, 8 ports
◆ PEX 8733: 32 lanes, 18 ports
◆ PEX 8732: 32 lanes, 8 ports
◆ PEX 8725: 24 lanes, 10 ports
◆ PEX 8724: 24 lanes, 6 ports
◆ PEX 8718: 16 lanes, 5 ports
◆ PEX 8717: 16 lanes, 10 ports
◆ PEX 8716: 16 lanes, 4 ports
◆ PEX 8714: 12 lanes, 5 ports
◆ PEX 8713: 12 lanes, 10 ports
◆ PEX 8712: 12 lanes, 3 ports

TECHNICAL SPECS

◆ Highly Flexible Port Configurations
◆ Lowest Power and Lowest Latency

CONTACT INFORMATION

PLX Technology, Inc
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40nm Superior Performance, Exclusive Feature-Rich Tools, DataCenter-Ready

◆ True Peer-to-Peer Data Transfer
◆ Hot-Plug Support

AVAILABILITY

PLX is the worldwide market leader with over 70 percent market share in PCIe switch products, today offering 18 ExpressLane™ PCIe Gen3 switches. The company has many more Gen3 switches in development to enable ExpressFabric, storage and other key data center applications, and in parallel is planning for PCIe Gen4 products.

APPLICATION AREAS

Data Center and Cloud Computing, Graphics, Industrial, Embedded

ExpressFabric® technology is a PLX initiative that utilizes the company’s next-generation PCIe switching devices to enable rack-level fabric capability for enterprise and cloud data center applications. Since virtually all devices – including host, communication, memory, special-purpose ASIC, and FPGA chips – have a direct connection to PCIe, the technology is a natural mechanism to provide converged connectivity inside the rack. By eliminating the bridging devices currently used to translate between the native PCIe device connections and protocols such as Ethernet and InfiniBand, a PCIe-based system can reduce latency and provide high performance with lower cost and substantial power savings. ExpressFabric technology is focused on operating within the rack, and can extend to medium-sized clusters with as many as 1000 nodes. While it may replace Ethernet and InfiniBand within the rack, it also can coexist and operate seamlessly with those technologies where they form the backbone of the data center outside the rack.

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Chip-to-Chip • 31
Teledyne LeCroy’s PCI Express® Protocol Analysis and Test Tools

Compatible Operating Systems: Windows XP/7/8
Specification Compliance: PCI Express Standards: 1.1, 2.0, and 3.0

Whether you are a test engineer or firmware developer, Teledyne LeCroy’s Protocol Analyzers will help you measure performance and quickly identify, troubleshoot and solve your protocol problems.

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The high performance Summit™ Protocol Analyzers feature the new PCIe virtualization extensions for SR-IOV and MR-IOV and in-band logic analysis. Decoding and test for SSD drive/devices that use NVM Express, SCSI Express and SATA Express are also supported.

Teledyne LeCroy offers a complete range of protocol test solutions, including analyzers, exercisers, protocol test cards, and physical layer testing tools that are certified by the PCI-SIG for ensuring compliance and compatibility with PCI Express specifications, including PCIe 2.0.

FEATURES & BENEFITS

◆ One button protocol error check. Lists all protocol errors found in a trace. Great starting point for beginning a debug session.
◆ Flow control screen that quickly shows credit balances for root complex and endpoint performance bottlenecks. Easily find out why your add-in card is underperforming on its benchmarks.
◆ LTSSM state view screen that accurately shows power state transitions with hyperlinks to drill down to more detail. Helps identify issues when endpoints go into and out of low power states.
◆ Full power management state tracking with Teledyne LeCroy’s Interposer technology. Prevents loosing the trace when the system goes into electrical idle.
◆ Teledyne LeCroy’s Data View shows only the necessary protocol handshaking ack/naks so you don’t have to be a protocol expert to understand if root complexes and endpoints are communicating properly.
◆ Real Time Statistics puts the analyzer into a monitoring mode showing rates for any user term chosen. Good for showing performance and bus utilization of the DUT.
◆ Zero Time Search provides a fast way to search large traces for specific protocol terms.

◆ Config space can be displayed in its entirety so that driver registers can be verified.

TECHNICAL SPECS

◆ Analyzer
  Lanes supported: X1,x2,x4,x8,x16
  Speeds: 2.5GT/s, 5GT/s and 8GT/s
  Probes/Interposers: active and passive PCIe slot, XMC, AMC, VPX, Express card, Express Module, Minicard, Mid-Bus, Multi-lead, External PCIe cable, CompactPCI, Serial SFF-8639, M.2/NGFF and others
  Form factor: Card, Chassis

◆ Exerciser
  Lanes supported: X1,x2,x4,x8,x16
  Speeds: 2.5GT/s, 5GT/s, 8GT/s
  Emulation: root complex and endpoint emulation

◆ Protocol Test Card
  Speeds: 2.5GT/s and 5GT/s operation
  Tests: Add-in-card test
  BIOS Platform Test
  Single Root IO Virtualization Test

APPLICATION AREAS

Mezzanine Boards, Add-in Cards, Host Carrier Systems, System Boards, Chips

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